MCS CCD 多通道式光谱感应器 - 卡尔蔡司 MCS CCD 系 光纤光谱感应器

MCS CCD 多通道式光谱感应器 (spectral sensor)系列一样，都是富弹性使用的设计，适用于各种应用光谱仪器感或设备内，符合各行各业的要求。这微型光纤光谱仪模块内所有元件在出厂前被石永久固定，元件结构包含：

(1)蔡司专利设计把陶瓷结构与检定的全息凹面光栅结合

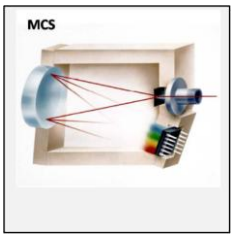
(2)光学输入口的设计包含光纤平面横切转换器或机械生产狭缝

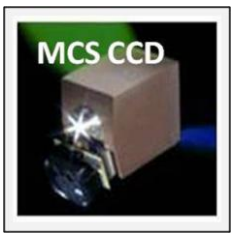
(3)电热冷冻 CCD 感测器(Hamamatsu detector) ，当中包含一个精密设计的 Peltier 元件，这更配备一个铜制散热风扇，这是分开供应的配件

(4) 另外你亦可选购前放大器

仪器的特点：

- 非常高灵敏性
- 适用低光源环境
- 满足多元测量，例如：荧光测量
- 稳健及高热稳定性强





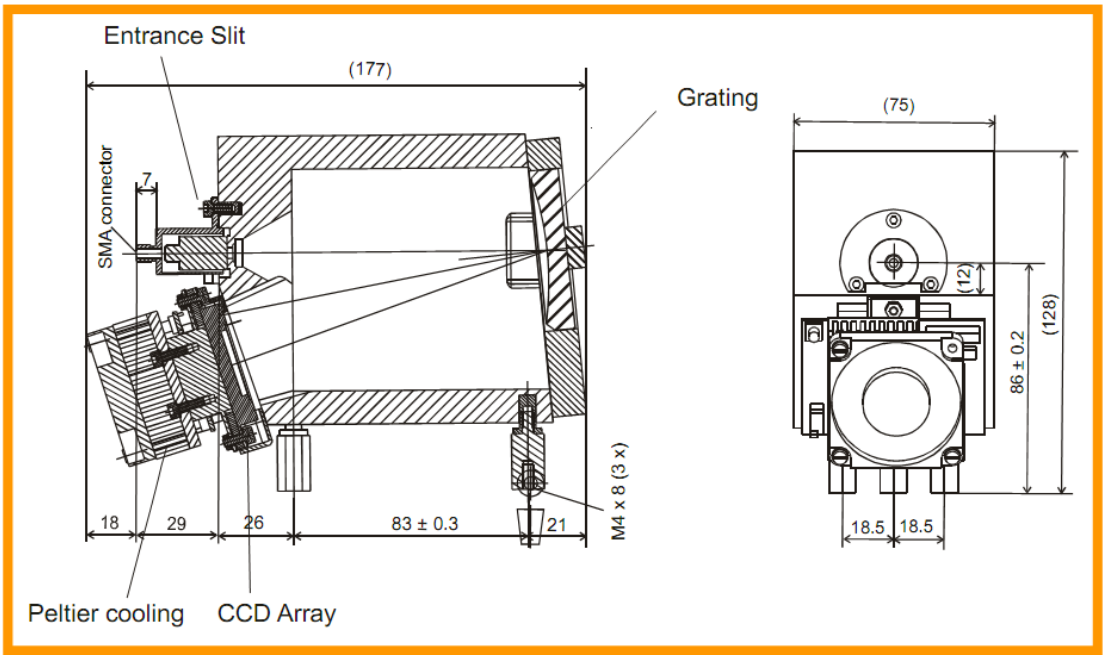
规格 SPECIFICATION

Model	**MCS CCD UV-NIR**	**MCS CCD UV**	**MCS CCD NIR**
Part No.	**000000-1212.556**	**000000-1212.555**	**On request**
Wavelength Range	200-980 nm	200-600 nm	600-980 nm
Optical Entrance			
input round	cross section converter, diameter: 0.5mm, NA = 0.22, mounted in SMA-coupling, dismountable		
output linear	70 µm x 1400 µm (optical entrance)		
Grating	Flat-field correction, 248 l/mm (center), blazed for approx. 250nm UV- version		
Wavelength accuracy absolute	< 0.5 nm		
Reproducibility	< 0,1nm		
Temperature - induced drift	< 0.01 nm/K		
Spectral distance of pixel	ΔλPixel ≈ 0.8 nm		
Resolution	Δλ ≤ 3 nm (UV-Version), Δλ = 3...4 nm (UV-NIR Version)		
Stray light	0.1% measured at 340 nm with Deuterium, lamp (transmission of NaNO2 solution, 50g/l, 1cm)		
Dimensions			
total (with case)	177 x 178x 75 mm^3		
Diode Array			
Brand	Hamamatsu		
Number of pixels	1024	512	512
Dimensions of pixels	24 x 24 µm²		
Maximum clock - rate	2 MHz		
System data			
Realized with	16-Bit-AD-conversion, integration time 10 ms, clock - rate 100 KHz and 50 cycles averaging		
Dynamic range			
Noise	1-2 counts standard deviation		

CCD Array

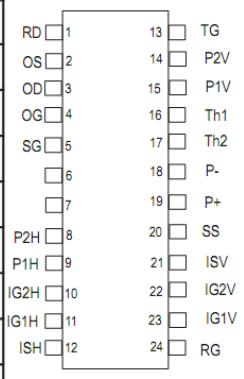
Producer:	Hamamatsu
Type:	S 7031-906 S 7031-1006
Number of pixels:	532 x 64 oder 1044 x 64
Dimensions of pixels:	24 x 24 µm²
Maximum clock – rate:	2 MHz

Blocking filter for the second order is directly coated on the CCD array.



Interface

PinNo.	Symbols	Function	Remarks	PinNo.	Symbols	Function	Remarks
1	RD	Reset Drain		13	TG	Transfer Gate	same pulse as 1'2V
2	os	Output Transistor Source		14	P2V	CCD Vertical Register Clock-2	
3	OD	Output Transistor Drain		15	P1V	CCD Vertical Register Clock-1	
4	OG	Output Gate		16	Thl	Thermistor	
5	SG	Summing Gate	same pulse as P211	17	Th2	Thermistor	
6	-			18	P-	Peltier-	
7	-			19	P`	Peltier'	
8	P2H	CCD Horizontal. Register Clock-2		20	SS	Substrate(GND)	
9	PIH	CCD Horizontal Register Clock-1		21	ISV	Test Point (Vertical Input Source)	connect to RD
10	IG2H	Test Point(Horizontal Input Gate-2)	conn ect. to OV	22	IG2V	Test Point (Vertical Input Gate-2)	connect to OV
11	1GIH	Test Point(Ilorizontal Input Gate-1)	connect to OV	23	IGIV	Test Point (Vertical Input Gate-1)	connect to OV
12	ISH	Test Point(1-lorizontal Input Source)	connect to RD	24	RG	Reset Gate	



System data

Realised with:	16-Bit-AD-conversion, tec 5 operating electronic, integration time 10 ms, 100 KHz and 50 cycles averaging
Dynamic range:	≥ 14 bit*

*= log 2 (FS/sdd), FS = full scale = max. signal, sdd= standard deviation(rms) of dark signal, 100 single readouts at 10 ms. The dynamic range can be enlarged by averaging.

Noise:	2...4 count standard deviation