

## Features

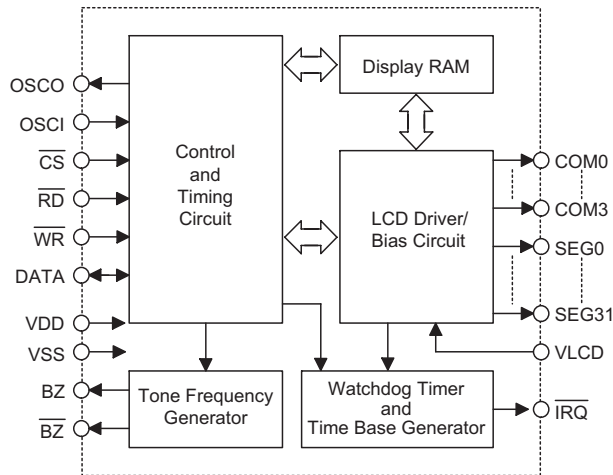
- Operating voltage: 2.4V~5.2V
- Built-in 256kHz RC oscillator
- External 32.768kHz crystal or 256kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32×4 LCD driver
- Built-in 32×4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage
- SHT32F21: 48-pin SSOP package
- SHT28D21: 28-pin SOP package
- SHT28C21: 28-pin SOP package
- SHT24F21: 24-pin SOP package
- 44-pin QFP package

## General Description

The SHT32F21 is a 128 pattern (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the SHT32F21 makes it suitable for multiple LCD applications including LCD modules and display sub-

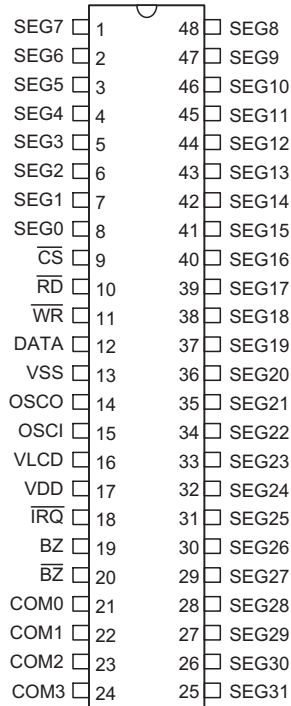
systems. Only three or four lines are required for the interface between the host controller and the SHT32F21. The SHT32F21 contains a power down command to reduce power consumption.

## Block Diagram

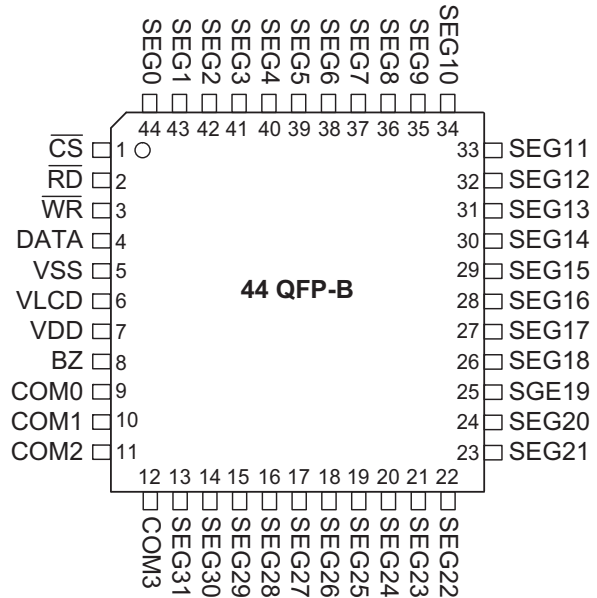


- Note:  $\overline{\text{CS}}$ : Chip selection  
 BZ,  $\overline{\text{BZ}}$ : Tone outputs  
 $\overline{\text{WR}}$ ,  $\overline{\text{RD}}$ , DATA: Serial interface  
 COM0~COM3, SEG0~SEG31: LCD outputs  
 $\overline{\text{IRQ}}$ : Time base or WDT overflow output

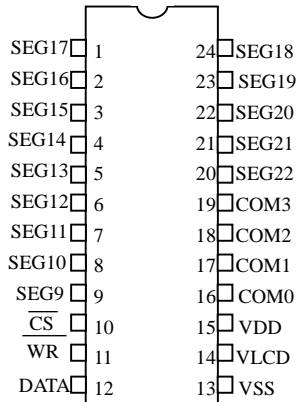
## Pin Assignment



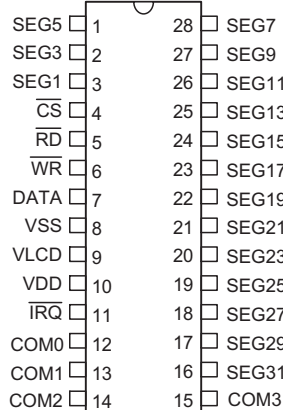
SHT32F21  
48 SSOP



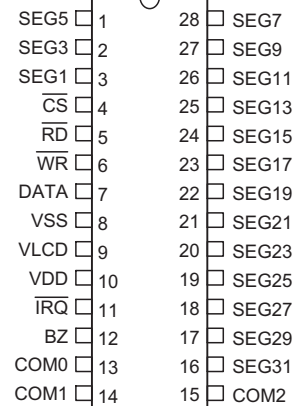
44 QFP-B



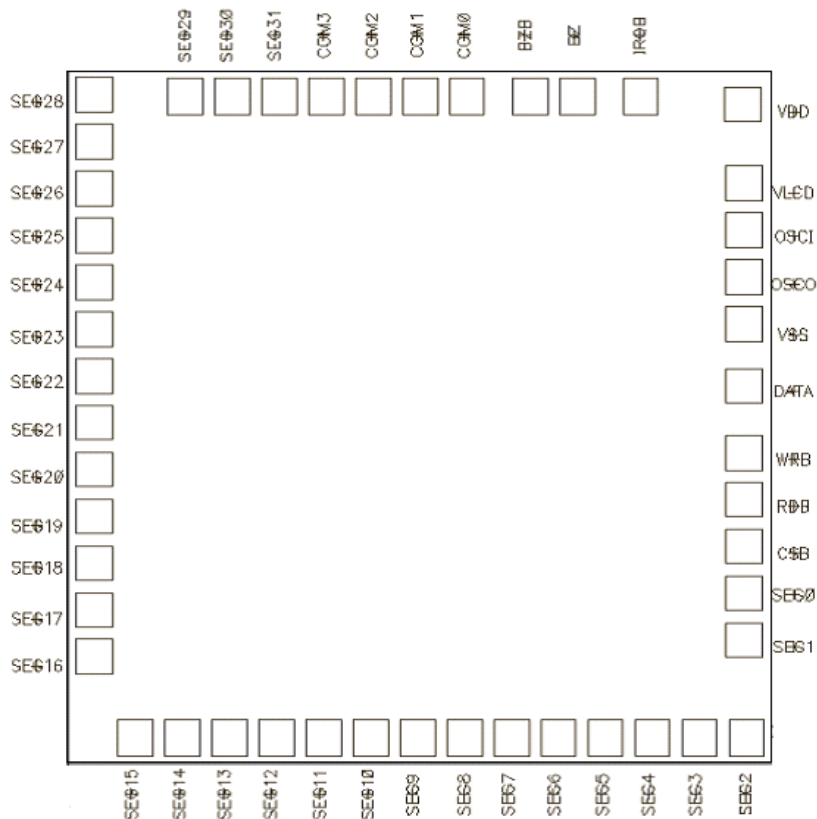
SHT24F21  
24 SOP



SHT28C21  
28 SOP



SHT28D21  
28 SOP



### Chip Size 1615\*1600(μ m)

PAD	NAME	X 坐标	Y 坐标	PAD	NAME	X 坐标	Y 坐标	PAD	NAME	X 坐标	Y 坐标
1	CSB	1554.5	501.6	17	SEG31	484.6	1538.5	33	SEG15	155	59.5
2	RDB	1554.5	609.6	18	SEG30	376.6	1538.5	34	SEG14	263	59.5
3	WRB	1554.5	717.6	19	SEG29	268.6	1538.5	35	SEG13	371	59.5
4	DATA	1554.5	871.7	20	SEG28	59.5	1543	36	SEG12	479	59.5
5	VSS	1554.5	1015.1	21	SEG27	59.5	1435	37	SEG11	587	59.5
6	OSC2	1554.5	1123.1	22	SEG26	59.5	1327	38	SEG10	695	59.5
7	OSC1	1554.5	1231.1	23	SEG25	59.5	1219	39	SEG9	803	59.5
8	VLCD	1554.5	1339.1	24	SEG24	59.5	1111	40	SEG8	911	59.5
9	VDD	1551.5	1520.9	25	SEG23	59.5	1003	41	SEG7	1019	59.5
10	IRQB	1315.8	1538.5	26	SEG22	59.5	895	42	SEG6	1127	59.5
11	BZ	1170.2	1538.5	27	SEG21	59.5	787	43	SEG5	1235	59.5
12	BZB	1062.2	1538.5	28	SEG20	59.5	679	44	SEG4	1343	59.5
13	COM0	916.6	1538.5	29	SEG19	59.5	571	45	SEG3	1451	59.5
14	COM1	808.6	1538.5	30	SEG18	59.5	463	46	SEG2	1559	59.5
15	COM2	700.6	1538.5	31	SEG17	59.5	355	47	SEG1	1554.5	285.6
16	COM3	592.6	1538.5	32	SEG16	59.5	247	48	SEG0	1554.5	393.6

PAD 坐标(X,Y)取 PAD 中心点,IC 以左下角为坐标原点

## Pad Description

Pad No.	Pad Name	I/O	Function
1	$\overline{CS}$	I	Chip selection input with pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the SHT32F21 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the SHT32F21 are all enabled.
2	$\overline{RD}$	I	READ clock input with pull-high resistor Data in the RAM of the SHT32F21 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the SHT32F21 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input/output with pull-high resistor
5	VSS	—	Negative power supply, ground
7	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
6	OSCO	O	
8	VLCD	I	LCD power input
9	VDD	—	Positive power supply
10	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output
11, 12	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
13~16	COM0~COM3	O	LCD common outputs
48~17	SEG0~SEG31	O	LCD segment outputs

## Absolute Maximum Ratings

Supply Voltage.....	$V_{SS}-0.3V$ to $V_{SS}+5.5V$	Storage Temperature.....	$-50^{\circ}C$ to $125^{\circ}C$
Input Voltage.....	$V_{SS}-0.3V$ to $V_{DD}+0.3V$	Operating Temperature.....	$-40^{\circ}C$ to $85^{\circ}C$

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
V <sub>DD</sub>	Operating Voltage	—	—	2.4	—	5.2	V
I <sub>DD1</sub>	Operating Current	3V	No load/LCD ON	—	150	300	μA
		5V	On-chip RC oscillator	—	300	600	μA
I <sub>DD2</sub>	Operating Current	3V	No load/LCD ON	—	60	120	μA
		5V	Crystal oscillator	—	120	240	μA
I <sub>DD3</sub>	Operating Current	3V	No load/LCD ON	—	100	200	μA
		5V	External clock source	—	200	400	μA
I <sub>STB</sub>	Standby Current	3V	No load, Power down mode	—	0.1	5	μA
		5V		—	0.3	10	μA
V <sub>IL</sub>	Input Low Voltage	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V <sub>IH</sub>	Input High Voltage	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I <sub>OL1</sub>	DATA, BZ, $\overline{BZ}$ , $\overline{IRQ}$	3V	V <sub>OL</sub> =0.3V	0.5	1.2	—	mA
		5V	V <sub>OL</sub> =0.5V	1.3	2.6	—	mA
I <sub>OH1</sub>	DATA, BZ, $\overline{BZ}$	3V	V <sub>OH</sub> =2.7V	-0.4	-0.8	—	mA
		5V	V <sub>OH</sub> =4.5V	-0.9	-1.8	—	mA
I <sub>OL2</sub>	LCD Common Sink Current	3V	V <sub>OL</sub> =0.3V	80	150	—	μA
		5V	V <sub>OL</sub> =0.5V	150	250	—	μA
I <sub>OH2</sub>	LCD Common Source Current	3V	V <sub>OH</sub> =2.7V	-80	-120	—	μA
		5V	V <sub>OH</sub> =4.5V	-120	-200	—	μA
I <sub>OL3</sub>	LCD Segment Sink Current	3V	V <sub>OL</sub> =0.3V	60	120	—	μA
		5V	V <sub>OL</sub> =0.5V	120	200	—	μA
I <sub>OH3</sub>	LCD Segment Source Current	3V	V <sub>OH</sub> =2.7V	-40	-70	—	μA
		5V	V <sub>OH</sub> =4.5V	-70	-100	—	μA
R <sub>PH</sub>	Pull-high Resistor	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	60	120	200	kΩ
		5V		30	60	100	kΩ

## A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
f <sub>SYS1</sub>	System Clock	—	On-chip RC oscillator	—	256	—	kHz
f <sub>SYS2</sub>	System Clock	—	Crystal oscillator	—	32.768	—	kHz
f <sub>SYS3</sub>	System Clock	—	External clock source	—	256	—	kHz
f <sub>LCD</sub>	LCD Clock	—	On-chip RC oscillator	—	f <sub>SYS1</sub> /1024	—	Hz
		—	Crystal oscillator	—	f <sub>SYS2</sub> /128	—	Hz
		—	External clock source	—	f <sub>SYS3</sub> /1024	—	Hz
t <sub>COM</sub>	LCD Common Period	—	n: Number of COM	—	n/f <sub>LCD</sub>	—	s
f <sub>CLK1</sub>	Serial Data Clock ( $\overline{WR}$ pin)	3V	Duty cycle 50%	4	—	150	kHz
		5V		4	—	300	
f <sub>CLK2</sub>	Serial Data Clock ( $\overline{RD}$ pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	
f <sub>TONE</sub>	Tone Frequency	—	On-chip RC oscillator	—	2.0 or 4.0	—	kHz
t <sub>CS</sub>	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	—	250	—	ns
t <sub>CLK</sub>	$\overline{WR}$ , $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	125	μs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	125	μs
			Read mode	3.34	—	—	
t <sub>r</sub> , t <sub>f</sub>	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	—	—	120	—	ns
t <sub>su</sub>	Setup Time for DATA to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 2)	—	—	—	120	—	ns
t <sub>h</sub>	Hold Time for DATA to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 2)	—	—	—	120	—	ns
t <sub>su1</sub>	Setup Time for $\overline{CS}$ to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 3)	—	—	—	100	—	ns
t <sub>h1</sub>	Hold Time for $\overline{CS}$ to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 3)	—	—	—	100	—	ns

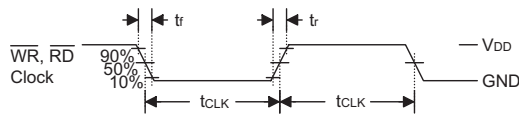


Figure 1

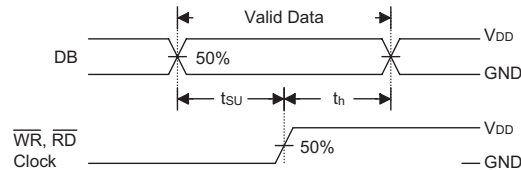


Figure 2

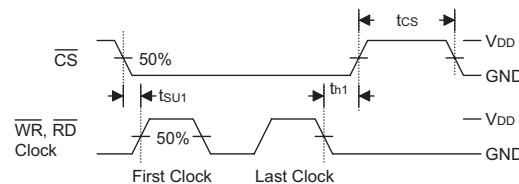
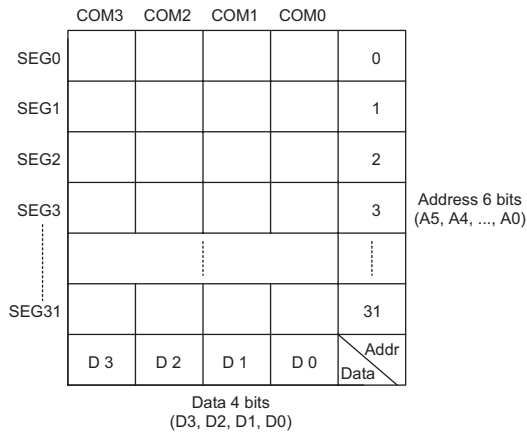


Figure 3

## Functional Description

### Display Memory – RAM

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:



**RAM Mapping**

### System Oscillator

The SHT32F21 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS

command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSC1 pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the SHT32F21 is at the SYS DIS state.

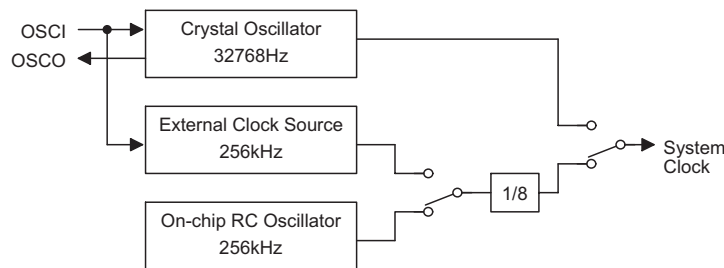
### Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the  $\overline{IRQ}$  output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

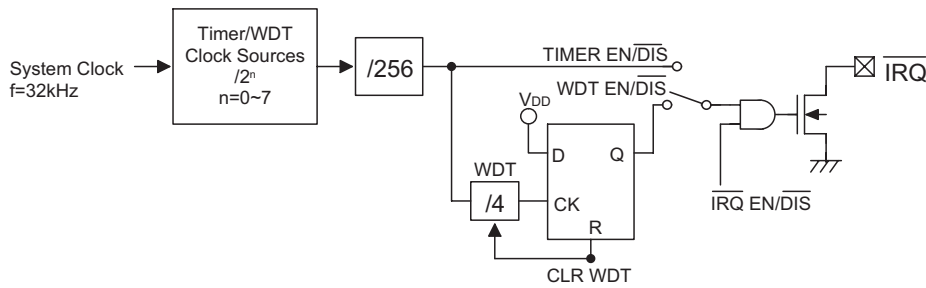
$$f_{WDT} = \frac{32kHz}{2^n}$$

where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz.

If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command



**System Oscillator Configuration**



### Timer and WDT Configurations

not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the  $\overline{\text{IRQ}}$  pin). After the **TIMER EN** command is transferred, the WDT is disconnected from the  $\overline{\text{IRQ}}$  pin, and the output of the time base generator is connected to the  $\overline{\text{IRQ}}$  pin. The WDT can be cleared by executing the **CLR WDT** command, and the contents of the time base generator is cleared by executing the **CLR WDT** or the **CLR TIMER** command. The **CLR WDT** or the **CLR TIMER** command should be executed prior to the **WDT EN** or the **TIMER EN** command respectively. Before executing the **IRQ EN** command the **CLR WDT** or **CLR TIMER** command should be executed first. The **CLR TIMER** command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the  $\overline{\text{IRQ}}$  pin will stay at a logic low level until the **CLR WDT** or the **IRQ DIS** command is issued. After the  $\overline{\text{IRQ}}$  output is disabled the  $\overline{\text{IRQ}}$  pin will remain at the floating state. The  $\overline{\text{IRQ}}$  output can be enabled or disabled by executing the **IRQ EN** or the **IRQ DIS** command, respectively. The **IRQ EN** makes the output of the time base generator or of the WDT time-out flag appear on the  $\overline{\text{IRQ}}$  pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the **SYS DIS** command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the SHT32F21 will continue working until system

power fails or the external clock source is removed. After the system power on, the  $\overline{\text{IRQ}}$  will be disabled.

### Tone Output

A simple tone generator is implemented in the SHT32F21. The tone generator can output a pair of differential driving signals on the **BZ** and **BZ**, which are used to generate a single tone. By executing the **TONE4K** and **TONE2K** commands there are two tone frequency outputs selectable. The **TONE4K** and **TONE2K** commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the **TONE ON** or the **TONE OFF** command. The tone outputs, namely **BZ** and **BZ**, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the **BZ** and the **BZ** outputs will remain at low level.

### LCD Driver

The SHT32F21 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the **S/W** configuration. This feature makes the SHT32F21 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 1 0 0, namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The **LCD OFF** command turns the LCD display off by disabling the LCD bias gen-

Name	Command Code	Function
LCD OFF	<b>1 0 0</b> 0 0 0 0 0 1 0 X	Turn off LCD outputs
LCD ON	<b>1 0 0</b> 0 0 0 0 0 1 1 X	Turn on LCD outputs
BIAS & COM	<b>1 0 0</b> 0 1 0 a b X c X	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option



erator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the SHT32F21 can be compatible with most types of LCD panels.

### Command Format

The SHT32F21 can be configured by the S/W setting. There are two mode commands to configure the SHT32F21 resources and to transfer the LCD display data. The configuration mode of the SHT32F21 is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
Read	Data	1 1 0
Write	Data	1 0 1
Read-Modify-Write	Data	1 0 1
Command	Command	1 0 0

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the  $\overline{CS}$  pin should be set to "1" and the previous operation mode will be reset also. Once the  $\overline{CS}$  pin returns to "0" a new operation mode ID should be issued first.

### Interfacing

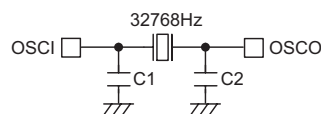
Only four lines are required to interface with the SHT32F21. The  $\overline{CS}$  line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the SHT32F21. If the  $\overline{CS}$  pin is set to 1,

the data and command issued between the host controller and the SHT32F21 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the SHT32F21. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The  $\overline{RD}$  line is the READ clock input. Data in the RAM are clocked out on the falling edge of the  $\overline{RD}$  signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the  $\overline{RD}$  signal. The  $\overline{WR}$  line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the SHT32F21 on the rising edge of the  $\overline{WR}$  signal. There is an optional  $\overline{IRQ}$  line to be used as an interface between the host controller and the SHT32F21. The  $\overline{IRQ}$  pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the  $\overline{IRQ}$  pin of the SHT32F21.

### Crystal Selection

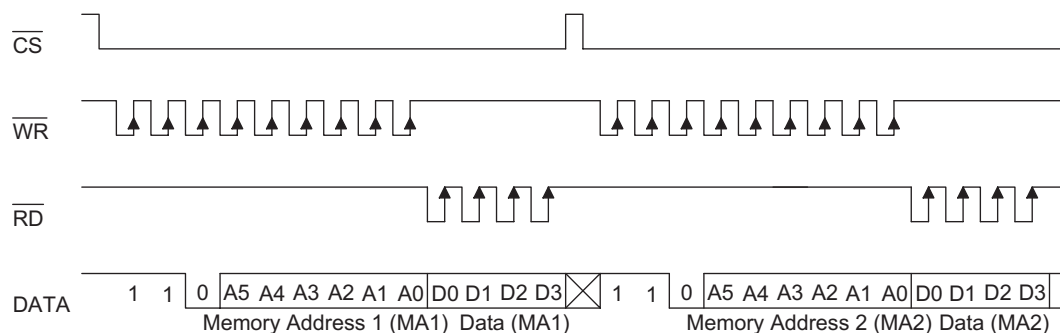
A 32768Hz crystal can be directly connected to the SHT32F21 via OSC1 and OSC0. In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table, which suggests the value of capacities. The table illustrates the suggestion value of capacities (C1, C2)

Crystal Error	Capacity Value
$\pm 10\text{ppm}$	0~10p
10~20ppm	10~20p

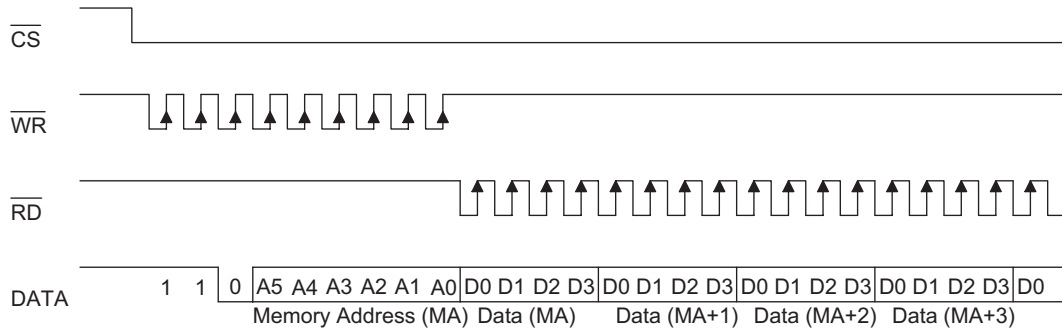


### Timing Diagrams

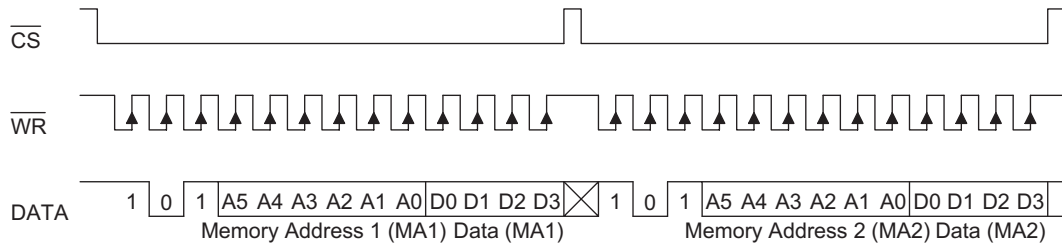
#### READ Mode (Command Code : 1 1 0)



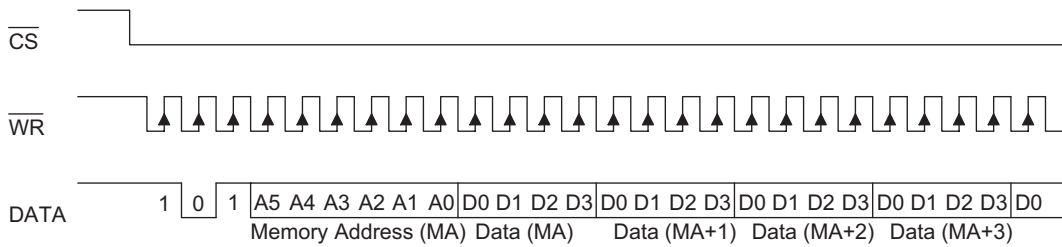
### READ Mode (Successive Address Reading)



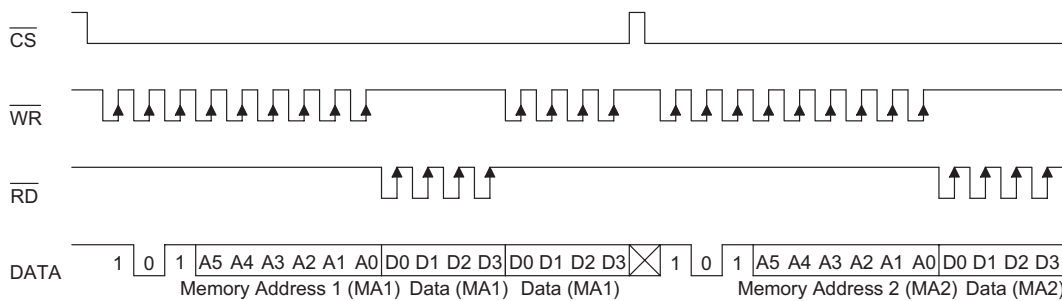
### WRITE Mode (Command Code : 1 0 1)



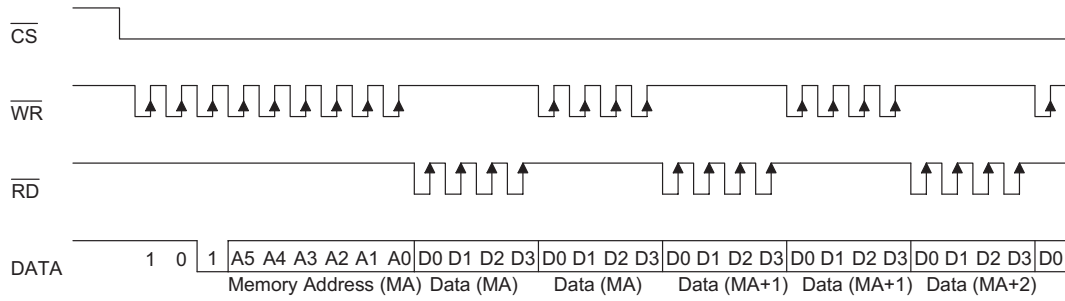
### WRITE Mode (Successive Address Writing)



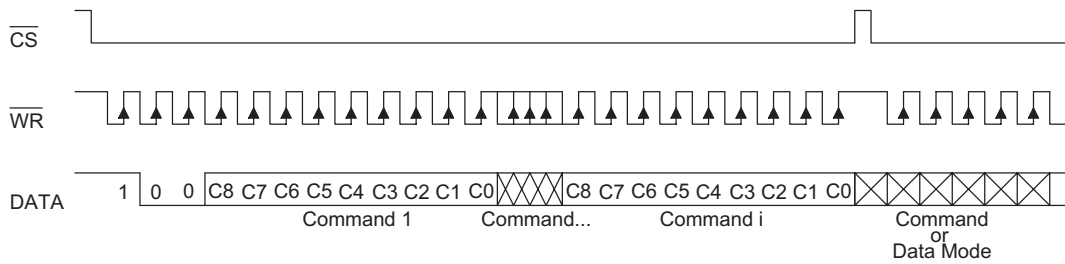
### Read-Modify-Write Mode (Command Code : 1 0 1)



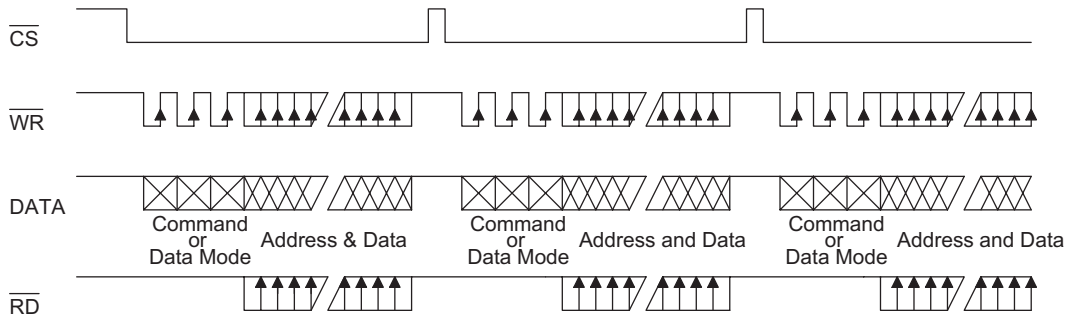
### Read-Modify-Write Mode (Successive Address Accessing)



### Command Mode (Command Code : 1 0 0)



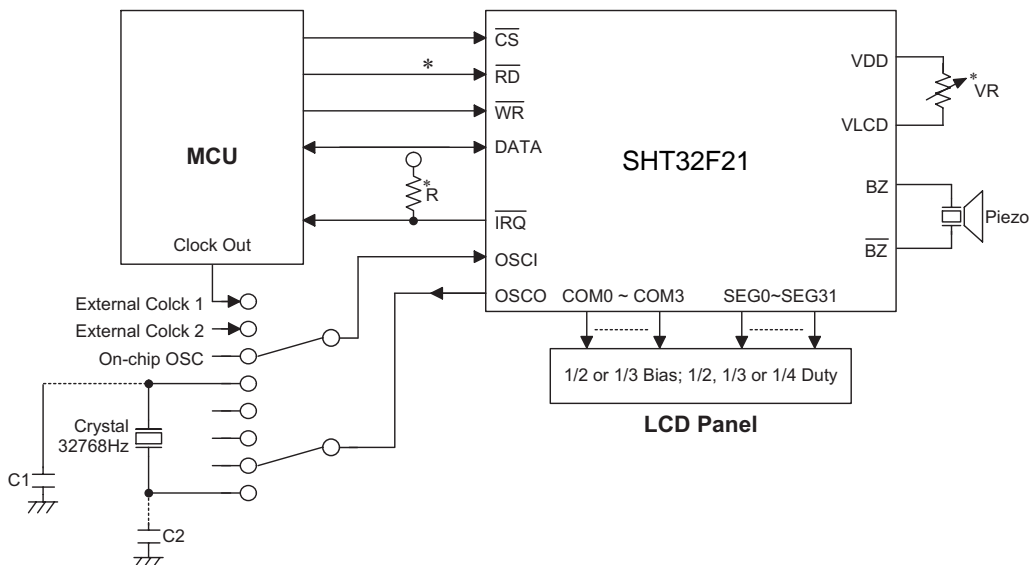
### Mode (Data and Command Mode)



Note: It is recommended that the host controller should read in the data from the DATA line between the rising edge of the  $\overline{RD}$  line and the falling edge of the next  $\overline{RD}$  line.

## Application Circuits

### Host Controller with an SHT32F21 Display System



Note: The connection of  $\overline{IRQ}$  and  $\overline{RD}$  pin can be selected depending on the requirement of the MCU.

The voltage applied to  $V_{LCD}$  pin must be lower than  $V_{DD}$ .

Adjust VR to fit LCD display, at  $V_{DD}=5V$ ,  $V_{LCD}=4V$ ,  $VR=15k\Omega\pm 20\%$ .

Adjust R (external pull-high resistance) to fit user's time base clock.

In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table, which suggests the value of capacities.

The table illustrates the suggestion value of capacities (C1,C2)

Crystal Error	Capacity Value
$\pm 10\text{ppm}$	0~10p
10~20ppm	10~20p

## Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	

Name	ID	Command Code	D/C	Function	Def.
TONE OFF	<b>1 0 0</b>	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	<b>1 0 0</b>	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	<b>1 0 0</b>	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	<b>1 0 0</b>	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	<b>1 0 0</b>	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	<b>1 0 0</b>	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	<b>1 0 0</b>	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	<b>1 0 0</b>	0010-abX0-X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1/3	<b>1 0 0</b>	0010-abX1-X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	<b>1 0 0</b>	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	<b>1 0 0</b>	011X-XXXX-X	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}}$ DIS	<b>1 0 0</b>	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	<b>1 0 0</b>	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	<b>1 0 0</b>	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	<b>1 0 0</b>	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	<b>1 0 0</b>	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	<b>1 0 0</b>	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	<b>1 0 0</b>	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	<b>1 0 0</b>	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	<b>1 0 0</b>	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	<b>1 0 0</b>	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	Yes
TEST	<b>1 0 0</b>	1110-0000-X	C	Test mode, user don't use.	
NORMAL	<b>1 0 0</b>	1110-0011-X	C	Normal mode	Yes

Note: X : Don't care

A5~A0 : RAM addresses

D3~D0 : RAM data

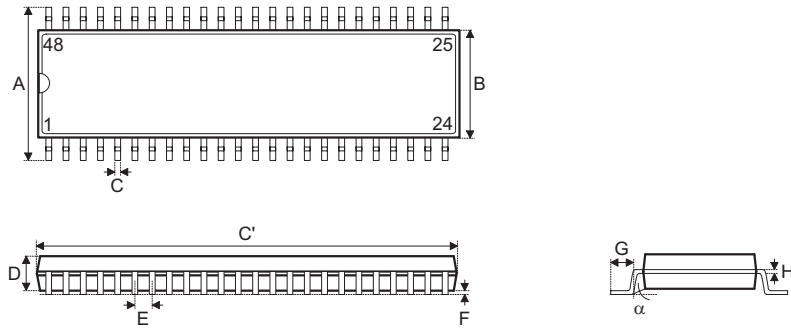
D/C : Data/command mode

Def. : Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the SHT32F21 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the SHT32F21.

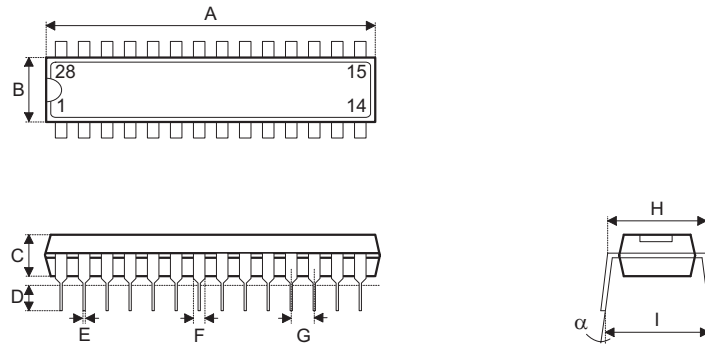
## Package Information

### 48-pin SSOP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	395	—	420
B	291	—	299
C	8	—	12
C'	613	—	637
D	85	—	99
E	—	25	—
F	4	—	10
G	25	—	35
H	4	—	12
$\alpha$	0°	—	8°

## 28-pin SKDIP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1375	—	1395
B	278	—	298
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	330	—	375
$\alpha$	0°	—	15°