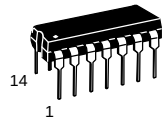
Description

The LM339 consists of four independent voltage comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply curr ent drain is independent of the magnitude of the power supply voltage. The outputs can be connected to other open -collector outputs to achieve wired -AND relationships.

Features

- Wide supply voltage range
- Low supply current drain independent of supply voltage.
- Low input biasing current
- Low input offset current
- Low input offset voltage
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage
- Output voltage compatible with TTL, MOS and CMOS logic



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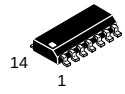
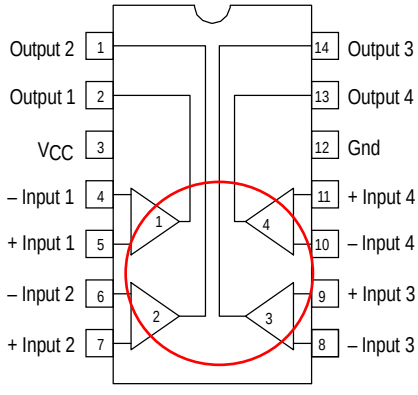


SOP – 14

Package

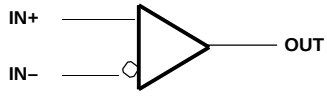
Internal Block Digram

PIN CONNECTIONS



(Top View)

symbol (each comparator)



Absolute Maximum Ratings

Symol	Parameter	Value	Unit
V_{CC}	Power Single Supply Split Supplies	 36 ±18	 V
V_{IDR}	Input Differential Voltage Range	36	V
V_{ICR}	Input Common Mode Voltage Range (1)	-0.3 to V_{CC}	V
t_S	Short-Circuit duration of Output	100	ms
	Input Current, per pin (2)	50	mA
T	perature Plastic Package	 150	 ℃
Tstg	Storage Temperature	-65 to +150	℃
T_L	Lead Temperature, 1mm from Case for 10 Seconds	260	℃
PD	Power Dissipation T_A=+25℃ Plastic Package Derate ℃	 1.0 8.0	 W mW/

*Maximum Ratings are those ues beyond which damage to the device may
Functional operation shouldbe restricted to the Recommended Operating Conditions.

1. Split Power
2. <-0.3V.

Switching

V_{CC}=5V, T_A=25℃

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5V through 5.1kΩ, C_L=15pF* (See	100-mV input step with 5 -mV overdrive		1.3		μs
		TTL-level input step		0.3		

* $C_L$includes probe and jig capacitance.

NOTE : The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

Electrical Characteristics

at specified free -air temperature, V_{CC} = 5V (unless otherwise noted)

PARAMETER	TEST CONDITIONS*			MIN	TYP	MAX	
V_{IO} Input offset voltage	V_{CC}=5V to 30V, $V_{IC} = V_{ICRmin}$, V_O=1.4V		25°C		2	5	mV
			Full range			9	
I_{IO} Input offset current	V_O=1.4V		25°C		5	50	nA
			Full range			150	
I_{IB} Input bias current	V_O=1.4V		25°C		-25	-250	
			Full range			-400	
V_{ICR} Common -mode input voltage range**			25°C	0 to Vcc-1.5			V
			Full range	0 to Vcc-2			
AVD Large -signal differential voltage amplification	V_{CC}=15V, V_O=1.4V to 11.4V, R_L 15kΩ to V_{CC}		25°C	50	200		V/mV
I_{OH} High -level output current	V_{OH}=5V, V_{ID}=1V		25°C		0.1	50	nA
	V_{OH}=30V, V_{ID}=1V		Full range			1	μA
VOL Low-level output voltage	I_{OL}=4mA, V_{ID}= -1V		25°C		150	400	mV
			Full range			700	
I_{OL} Low-level output current	V_{OL}=1.5V, V_{ID}= -1V		25°C	6			mA
ICC Supply current	R_L=	V_{CC}=5V	25°C		0.8	2	mA
		V_{CC}=30V	Full range			2.5	

* Full range (MIN to MAX), for the LM339 is 0°C to 70 °C. All characteristics are measured with zero common -mode input voltage unless otherwise specified.

** The voltage at either input or common -mode should not be allowed to go negative by more than 0.3 V. The upper end of the common -mode voltage range is V_{CC} -1.5 V, but either or both inputs can go to 30 V without damage.

Typical Performance Characteristics

(V_{CC} =1.5V, T_A=+25°C (each

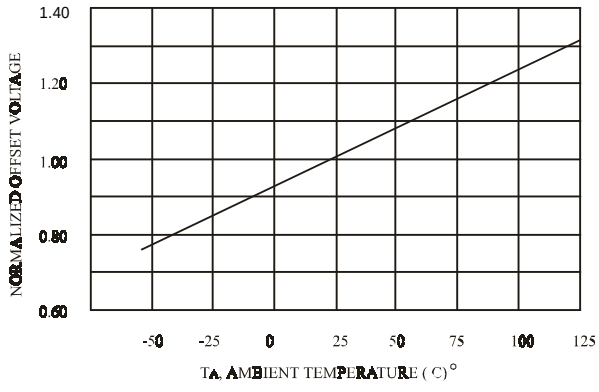


Figure 1. Normalized Input Offset Voltage

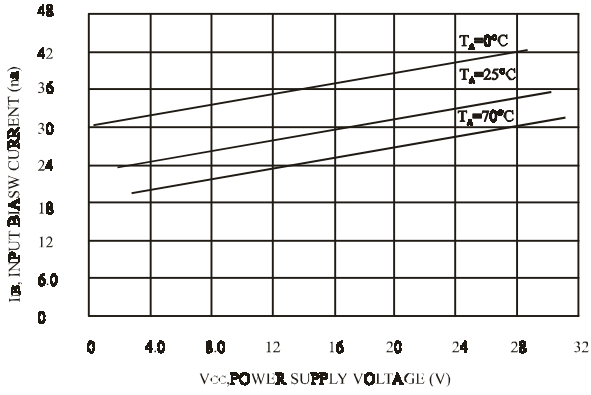


Figure 2. Input Bias Current

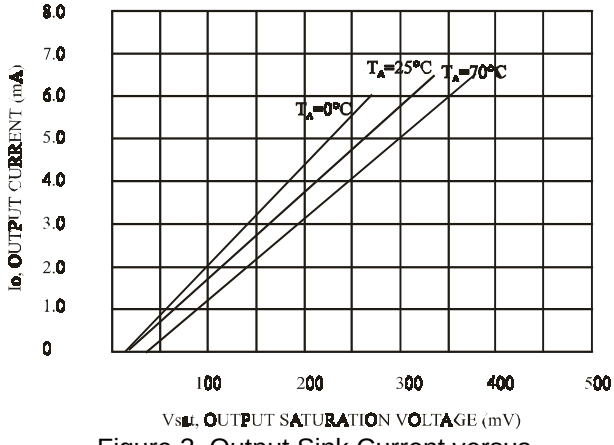


Figure 3. Output Sink Current versus Output Saturation Voltage

Typical Applications Circuit

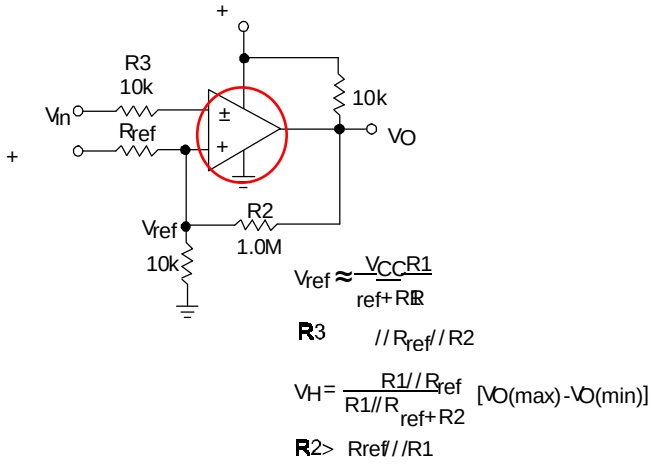


Figure 11. Inverting with Hystersis

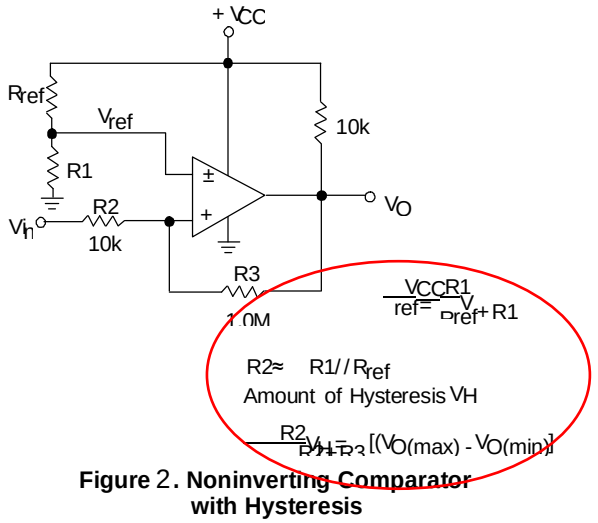
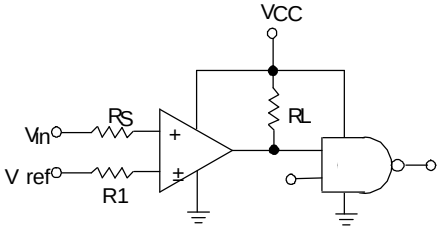


Figure 2. Noninverting Comparator with Hysteresis



RS = Source Resistance
R1 ≈ RS

Logic	Device	VCC (V)	RL kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 3. Driving Logic

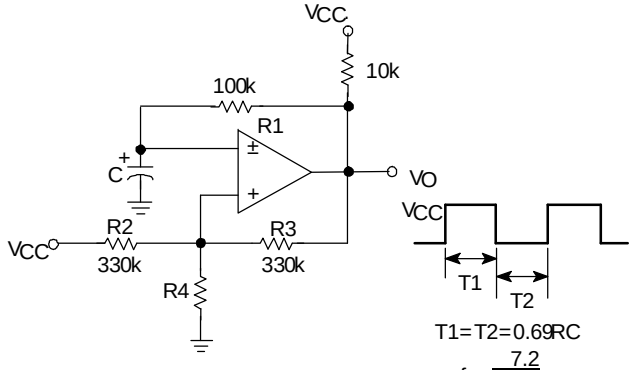
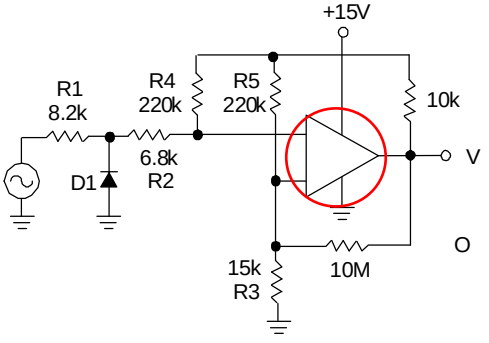


Figure 4. Squarewave Oscillator



D1 prevents input from going negative by more than 0.6 V

R1+R2=R3

$R3 \frac{R5}{10}$ forsmallerroiinzerocrossing

Figure 5. Zero Crossing Detector

$V_{in(min)} \approx 0.4V$ Peak for 1% phase distortion ($\Delta\Theta$).

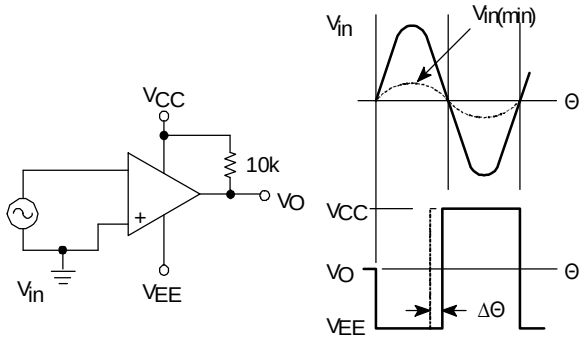


Figure 6. Zero Crossing Detector

Ordering Information

ORDERING NUMBER	PACKAGE	MARKING
LM339M	SOP-14 /DIP-14	LM339