ESD association standard test method

ANSI/ESD STM5.1-2001

ANSI/ESD STM5.1-2001

For Electrostatic Discharge Sensitivity Testing

Human Body Model (HBM) Component Level

Electrostatic Discharge Association
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ESD STM5.1-1998

ESD Association Standard Test Method for electrostatic discharge sensitivity testing –

Human Body Model (HBM) Component Level

Approved May 20, 2001
ESD Association

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Foreword

To characterize a component's electrostatic discharge (ESD) susceptibility fully, it should be tested to the following three ESD test standards:

- Human Body Model (HBM)
- Charged Device Model (CDM)
- Machine Model (MM)

Requirements for MM and CDM testing are contained in ESD Association Standard Test Methods STM 5.1 and STM5.3.1 respectively.

Users of this standard test method should understand that the data obtained when classifying components does not necessarily mean that the components will be unaffected if subjected to a lower level of actual electrostatic discharge (ESD). ESD from a human being varies considerably, and depends on many factors. Some of these variable factors include: the characteristics of the individual human body; proximity to a ground plane or other objects; whether the discharge occurs from a finger or a hand-held metal object; and t5he coupling between the component and ground.

The waveform specified in this standard test method is similar to that of MIL-STD-883D Method 3015.7, but the characteristic and ESD stress test method is further defined. Existing data, generated with testers meeting the waveform specifications contained here, shall be considered valid ESD stress test data in accordance with this standard test method.

This updated standard test method contains non-technical changes and is an updated version of the ED-STM5.1-1998 that was originally approved on February 8, 1998. This standard test method was processed and approved for reaffirmation to the ESD Association Standards Committee (STDCOM). At the time that this standard test method was approved the working group had the following members:

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ESD Association Standard Test Method for electrostatic discharge sensitivity testing.

HUMAN BODY MODEL (HBM) - Component Level

1. Scope and purpose

1.1 Scope

This standard establishes the procedure for testing, evaluating, and classifying the electrostatic discharge (ESD) sensitivity of components to the defined human body model (HBM).

1.1.1 Existing data

Data previously generated with testers meeting all waveform criteria of this standard shall be considered valid test data.

1.2 Purpose

The purpose of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable results from tester to tester, regardless of component type. Repeatable data will allow accurate comparisons of HBM ESD sensitivity levels.

2. References

ESD ADV. 1.0 Glossary of Terms[1]
EOS/ESD - S 5.1 (previous HBM issues)
EOS/ESD - S 5.2 Machine Model (MM)
ESD - S5.2 MM

3. Definitions

The following definitions are in addition to those in the EOS/ESD Glossary of Terms.

3.1 Component

An item such as a resistor, diode, transistor, integrated circuit or hybrid circuit.

[1] ESD Association, 7900 Turin Road, Bldg 3, Ste 2, Rome, NY 13440, 315-339-6937

3.2 Component failure

A condition in which a tested component does not meet one or more specified static or dynamic data sheet parameters.

3.3 Data sheet parameters

Static and dynamic component performance data supplied by the component manufacturer or user.

3.3.1 Static parameters are those measured with the component in a non-operating condition. These may include, but are not limited to: input leakage current, input breakdown voltage, output high and low voltages, output drive current, and supply current.

3.3.2 Dynamic parameters are those measured with the component in an operating condition. These may include, but are not limited to full functionality, output rise and fall times under a specified load condition, and dynamic current consumption.

3.4 Electrostatic discharge sensitivity (ESDS)

The ESD level that causes component failure.

3.5 ESD withstand voltage

The maximum ESD level that does not cause component failure.

3.6 Human body model (HBM) ESD

An ESD event meeting the waveform criteria specified in this standard, approximating the discharge from the fingertip of a typical human being.

3.7 Machine Model (MM) ESD

An ESD event meeting the criteria specified in the Machine Model standard S5.2.

3.8 HBM ESD tester

Equipment (referred to as "tester" in this standard) that applies Human Body Model ESD to a component.

3.9 Ringing

High frequency oscillation superimposed on the waveform.

3.10 Step stress test hardening

This occurs when a component subjected to increasing ESD voltage stresses is able to withstand higher stress levels than a similar component stressed at a single lower voltage level. For example: a component may fail at 1000 volts if subjected to a single stress, but fail at 3000 volts if stressed incrementally from 250 volts.

4. HBM ESDS Component classifications

ESD sensitive components are classified according to their HBM ESD withstand voltage, regardless of polarity. The HBM ESDS component classification levels are shown in Table 1.

Table 1 HBM ESDS Component Classification

Class	Voltage Range
0	< 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

5. Required equipment

5.1 HBM ESD tester

An acceptable ESD tester is composed of equipment meeting the requirements of this standard. (Schematically represented in Figure 1, producing pulses meeting the waveform characteristics specified in Figures 2 and 3.)

5.2 Waveform verification equipment

Equipment capable of verifying the pulse waveforms defined in this standard include but is not limited to an oscilloscope, two evaluation loads, and a current transducer.

5.2.1 Oscilloscope requirements:

a. Minimum sensitivity of 100 milliampere per major division (typically one centimeter) when used in conjunction with the current transducer specified in Section 5.2.3.

b. Minimum single shot bandwidth of 350 megahertz.

c. Minimum writing rate of one major division per nanosecond.

5.2.2 Evaluation loads. Two evaluation loads are necessary to verify tester functionality:

a. Load 1: A solid 18-24 AWG (0.83 to 0.21 mm^2 cross-section) tinned copper shorting wire as short as practicable to span the distance between the two farthest pins in the socket while passing through the current probe.

b. Load 2: A 500 ohm, ±1%, 1000 volt, low inductance, sputtered film resistor (Caddock Industries type MG 714 or equivalent).

5.2.3 Current transducer requirements:

a. Minimum bandwidth of 350 megahertz.

b. Peak pulse capability of 12 ampere.

c. Rise time of less than 1 nanosecond.

d. Capable of accepting a solid conductor of 1.5 millimeters in diameter.

e. Provide an output voltage per milliampere as required in section 5.2.1.a. (Usually between one and five millivolt per milliampere.)

A Tektronix CT-1 or equivalent with a maximum cable length of 1 meter meets these requirements.

6. Equipment and waveform requirements

6.1 Equipment calibration

All equipment used to evaluate the tester shall be periodically calibrated in accordance with the manufacturer's recommendation. This includes the oscilloscope, current transducer, and high voltage resistor load. Maximum time between calibrations is one year. Calibration shall be traceable to national standards, such as the National Institute of Standards and Technology (NIST) in the United States, or comparable international standards.

6.2 Tester qualification and requalification

HBM ESD tester initial qualification in accordance with Section 7 shall be performed as part of the acceptance testing when the ESD tester is delivered or first used.

Perform the HBM ESD tester requalification described in Section 7.1 in accordance with the manufacturer's recommendation. Maximum time between full requalification tests is one year. Perform tester verification in accordance with

Section 7.3 following repairs or servicing that could affect the waveform. Use the highest pin count test fixture board with a positive clamp socket for the waveform verification. All other test fixture boards shall be checked routinely when they are used in accordance with Section 8.1.2.

Note 1: A positive clamp test socket is a zero insertion force (ZIF) socket with a clamping mechanism. It allows the shorting wire to be easily clamped into the socket. Examples are dual in-line package (DIP) and pin grid array (PGA) ZIF sockets.

6.3 Tester waveform records

6.3.1 Tester waveform records: new equipment

Record positive and negative waveforms (using either photographs or digitized waveforms) during the tester initial qualification procedures. Test each socket in accordance with Section 7.1. Use the voltage levels defined in Section 7.2. Retain the waveform records until the next calibration or for the duration specified by the internal record keeping procedures.

6.3.2 Tester waveform records: old equipment. Record positive and negative using both the short circuit wire and the 500 ohm load resistor as defined in Section 7.1. Use the highest pin count test fixture with a positive clamp socket. Perform these tests as recommended by the equipment manufacturer or during the yearly calibration cycle. Retain the waveform records until the next calibration or for the duration specified by the internal record keeping procedures.

7. Qualification and verification procedures

7.1 HBM ESD tester and test fixture board qualification procedure

HBM ESD tester qualification shall ensure waveform integrity of the peak current into a short (Ips) as specified in Figures 2a, 2b and 3. For initial qualification, qualify each socket on the test fixture board.

For tester requalification, it is only necessary to use the highest pin count text fixture board with a positive clamp socket. All other positive clamp test fixture boards shall be checked when they are used in accordance with Section 8.1.2.

7.1.1 Verify electrical continuity for all pins on the test fixture board.

7.1.2 Qualification of new test fixture boards

7.1.2.1 For each socket identify the socket pin with the shortest wiring path to the pulse generation circuit. Connect this pin to Terminal B**.** Connect each of the other pins in turn to Terminal A. Apply a ± 1000 volt pulse using the shorting wire. All waveform parameters shall be within the limits specified in Figure 2a and Figure 3.

7.1.3 Qualification of existing test fixture boards

7.1.3.1 Define the reference pin pair for each test socket on the test fixture board. Identify the socket pin with the shortest wiring path from the pulse generation circuit to the test socket. Connect this pin to Terminal B. Identify the pin with the longest wiring path from the pulse generator circuit to the ESD stress socket. Connect this pin to Terminal A.

Alternatively, the reference pin pair previously identified during MM testing may be used. (Refer to ESD-S5.2)

7.1.3.2 Attach the shorting wire between the reference pin pair connected to Terminal A and Terminal B. Place the current transducer around the shorting wire, as close to Terminal B as practical, observing the polarity shown in Figure 1.

a. For positive clamp sockets, insert the shorting wire between the socket pins connected to Terminals A and B.

b. For non-positive clamp sockets, attach the shorting wire to the wiring of the test

fixture between the socket pins connected to Terminals A and B. The connection points shall be as close as possible to the test socket pins.

7.1.3.3 Apply 5 positive and 5 negative pulses. Observe waveforms at 1000 volts, 2000 volts, and 4000 volts. Verify that the waveforms meet all parameters specified in Figure 2a.

7.1.3.4 Replace the shorting wire with the 500 ohm resistor. Pass the wire end of the resistor that will be connected to Terminal B through the current transducer observing the polarity shown in Figure 1.

7.1.3.5 Observe waveforms at 1000 and 4000 volts, both positive and negative polarities. Verify that the waveforms meet all parameters specified in Figure 3.

7.1.3.6 Set the horizontal time scale of the oscilloscope to one millisecond per division. Using the shorting wire, initiate a pulse and verify that any spurious pulse is less than 15% of the amplitude of the main pulse.

7.2 Waveform verification procedure

Use the following procedure to verify the waveforms.

7.2.1 Verify electrical continuity for all pins on the test socket fixture board.

7.2.2 Attach the shorting wire between the reference pin pair. Place the current transducer around the shorting wire, as close to Terminal B as practical, observing the polarity shown in Figure 1.

7.2.3 Use the shorting wire to verify the waveforms at 1000 and 4000 volts (or for the stress level to be tested), for both positive and negative polarities. Verify the waveforms at 8000V if testing will be performed above 4000V. Verify that the waveforms meet all parameters specified in Figure 2a.

7.2.4 Set the horizontal time scale of the oscilloscope to one millisecond per division. Initiate a pulse and verify that any spurious pulse is less than 15% of the amplitude of the main pulse.

7.3 Waveform verification following servicing

Verify the waveforms meet all parameters specified in Figure 2a after any repairs or servicing of the tester following manufacturer's recommendations and Section 7.1.

8. ESDS testing requirements and procedures

8.1 Test requirements

8.1.1 Handling of components. Use ESD damage prevention procedures when handling components before, during and after testing.

8.1.2 Required waveform check. Verify waveform integrity (described in Section 7.2) using the shorting wire at ±1000 volts, or the stress level to be tested. Waveform integrity shall be checked for the reference pin pair as designated in Section 7.1.3.

The waveform check is required for positive clamp sockets each time the test fixture board is changed. The waveform check is recommended for all other socket types.

Verify the waveform at least once per shift. If necessary, remove the test fixture board being used and replace with a positive clamp socket test fixture board to facilitate waveform measurements. Longer periods between waveform checks may be used if no changes in waveforms are observed for several consecutive checks. However, if the waveforms no longer meet the specified limits, all ESD stress tests subsequent to the previous satisfactory waveform check shall be considered invalid.

If ESD stress testing is performed in consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

8.1.3 High voltage discharge path check. Test the high voltage discharge path and all associated circuitry at the beginning of each day during which ESD stress testing is performed. Use the tester manufacturer's recommended procedure. If any failure is detected, do not perform testing with the sockets that use the defective discharge paths. Repair the tester and then requalify it in accordance with Section 7.3.

8.1.4 Component static and dynamic tests. To determine whether components have failed, perform static and dynamic testing to all data sheet parameters before and after ESD testing. Pin leakage current may only be used as guides in determining the component ESD withstand

voltage. It is not sufficient, especially for complex integrated circuits, to use pin leakage as the only criterion for component failure.

8.1.5 Pin combinations.

The pin combinations to be used for ESD stressing of all integrated circuit components are given in Table 2 and Section 8.1.5.1. Pin combination (n) is the total number of pin combinations. This varies from component to component depending on the number of power pin groups with the same name. Vps(i) in table 2, is any set of like named power supply or ground pins (e.g., Vcc, Vss, Vdd, analog GND, digital GND, etc.) which are metallically connected (within 2 ohms) on the chip or within the package. Like named pins that are resistively connected via the chip substrate or wells, or are electrically isolated from each other (more than 2 ohms), are considered separate sets for the purpose of these tests. (i.e., if two pins are labeled Vcc, but are not metallically connected within 2 ohms within the chip/package, they shall be treated as distinct and separate Vps(i) sets.) Only those pins that supply current to or interface to other pins shall be considered to be power pins. Pins such as Vcc, Vdd, GND, Vss, Vee, +Vs and -Vs are considered power supply pins. These pins supply current to input and output buffers in such a way as to interface closely with the environment through other pins.

Pins such as offset adjust, compensation, clocks, controls, address, data, Vref, no connects (NC), output and input pins are considered non-power supply pins. For example, a programming power pin, usually called Vpp, shall be considered to be a non-power supply pin because it does not supply current to or interface with any other pins, and is not a diode drop away from any non-power pins.

For further clarification on pin combinations, see example in Appendix A.

Pin combinations to be used for ESD stressing of all active and passive discrete components and component arrays are given in Section 8.1.5.1.

8.1.5.1 Pin combinations for all discrete components and component arrays (including both passive and active components).

All possible pin pair combinations (one pin to terminal A, another to terminal B) regardless of pin function.

Table 2-Pin combinations for all digital, analog and hybrid integrated circuits

Pin Combination Set	Connect Individually to Terminal A	Connect to Terminal B (Ground)	Floating Pins (unconnected)
1	All pins one at a time, except the pin(s) connected to terminal B	Vps(1) [First power pin(s)]	All pins except pin under test (PUT) and Vps(1) [First power pin]
2	All pins one at a time, except the pin(s) connected to terminal B	Vps(2) [Second power pin(s)]	All pins except PUT and Vps(2)[Second power pin]
i	All pins one at a time, except the pin(s) connected to terminal B	Vps(i) [ith power pin(s)] [1,2, ...i]	All pins except PUT and Vps(i)
n-1	All pins one at a time, except the pin(s) connected to terminal B	Vps(n-1)	All pins except PUT and Vps(n-1)
n	All non-Vps(i) pins one at a time.	All other non-Vps(i) pins, except the pin connected to terminal A.	All Vps(i) pins

8.2 HBM classification and ESD stress testing procedure

Classify components according to their HBM ESD withstand voltage. Perform ESD stress testing at room temperature in accordance with the procedure below. It is permissible to use any voltage level in Table 3 as the starting stress level. Three new components may be used at each voltage level or pin combination if desired. This will eliminate any step stress hardening effects, and reduce the possibility of early failure due to cumulative stress on power pins. However, if a single set of three components is stressed at each level, then to avoid missing possible ESD vulnerability windows, it is recommended not to miss any stress step.

ESD classification testing shall be considered destructive to the component, even if no component failure occurs.

Table 3 HBM ESD Stress Levels

Stress Level	Equivalent Charging (±) voltage Vp (volt)
1	250
2	500
3	1000
4	2000
5	4000
6	8000 (optional)

Note 2: A component may pass at 4000V but fail at 2000V; this is called a component fail window. To avoid this fail window, it is recommended that components are tested at each classification level defined in Table 3.

Use the following procedure to classify components:

8.2.1 Test a minimum of three samples of the component to all specified static and dynamic data sheet parameters.

8.2.2 Determine the starting stress voltage level from Table 3. Select the first pin combination to be tested as stated in Section 8.1.5.

8.2.3 Apply one positive and one negative pulse to the component. Allow at least a 0.3 second interval between pulses. Repeat this process using all other pin combinations specified in Section 8.1.5.

Note 3: One pulse per polarity is a significant change from previous 5.1 HBM standards (1991, 1993), which were three pulses per polarity.

8.2.4 Test the components to full static and dynamic data sheet parameters and record the results for each component. Parametric and functional testing shall be performed at room temperature. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.

If all three components pass the specified data sheet parameters, repeat steps 8.2.3 through 8.2.4, using the next higher stress level of Table 3. Three new components may be used at each voltage level or pin combination if desired.

8.2.5 If one or more components fail, repeat the ESD stress test using three new components starting at the next lower stress level. If the components continue to fail, decrease the stress voltage until level 1 is reached in Table 3. If any additional failures are observed at level 1, stop all testing at this level.

9. Failure criteria

A component is considered an ESD failure if it fails the data sheet parameters as specified in section 8.2.4.

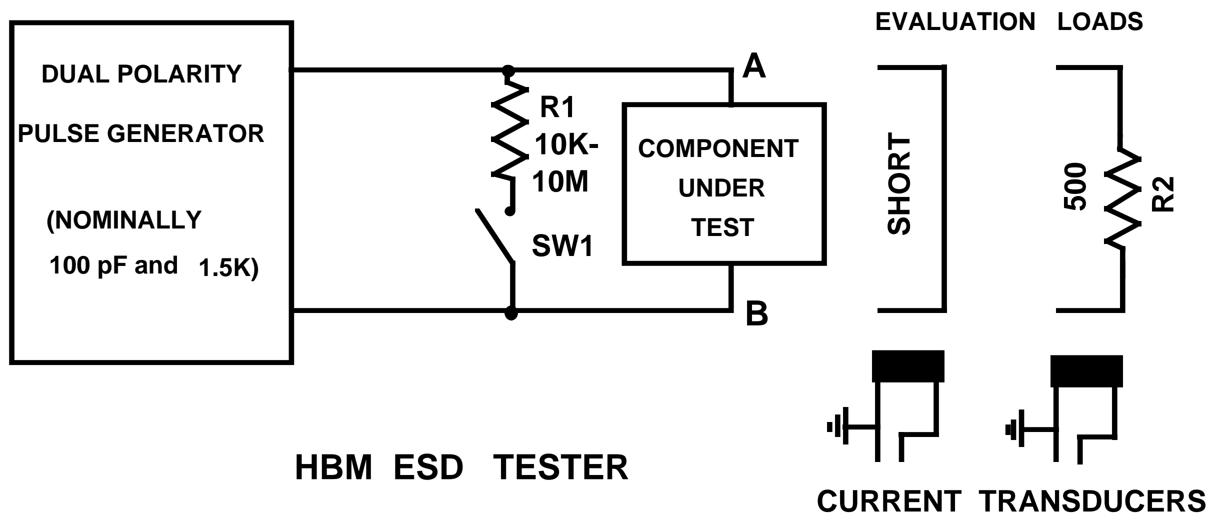


Figure 1-ESD stress test (HBM)

Requirements:

1. The current transducers are specified in 5.2.3
2. The shorting wire and 500 ohm resistor R2 are specified in 5.2.2
3. Reversal of Terminals A and B to achieve dual polarity performance is not permitted.
4. SW1 is closed 10 to 100 milliseconds after the pulse delivery period to ensure the socket is not left in a charged state. It should be opened at least 10 milliseconds prior to the delivery of the next pulse. The resistance R1 in series with the switch ensures a slow discharge of the device, thus avoiding the possibility of a charged device model discharge.
5. The Dual Polarity Pulse Generator shall be designed to avoid recharge transients and double pulses.
6. Piggybacking of test sockets (the insertion of secondary sockets into the main test socket) is allowed only if the secondary socket waveform meets the requirements of this standard.
7. Measure the current waveform as described in Section 7.2.

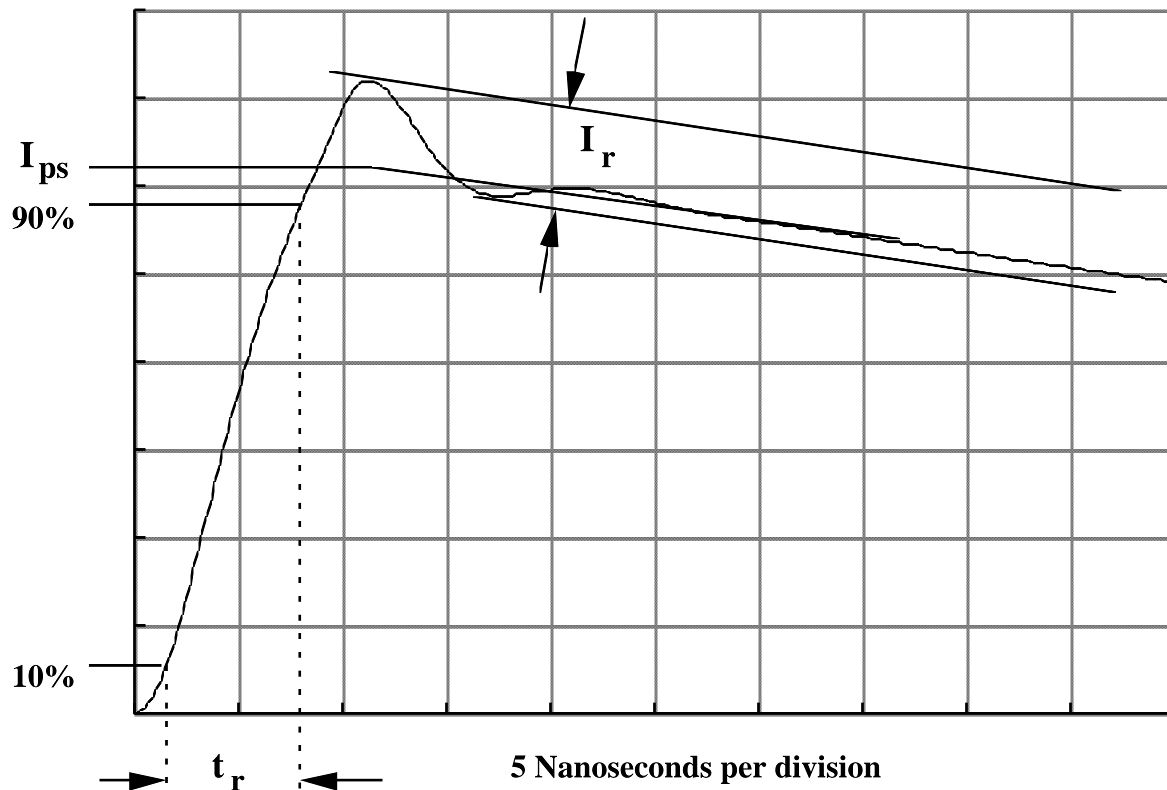


Figure 2a-Current pulse through a shorting wire

Parameter	Value
I_{PS} for 250V stress (ampere)	0.17 (±10%)
I_{PS} for 500V stress (ampere)	0.33 (±10%)
I_{PS} for 1000V stress (ampere)	0.67 (±10%)
I_{PS} for 2000V stress (ampere)	1.33 (±10%)
I_{PS} for 4000V stress (ampere)	2.67 (±10%)
I_{PS} for 8000V stress (ampere) (**4**)	5.33 (±10%)
t_r (pulse rise time)	2 to 10 nanoseconds
I_r (peak to peak ringing)	< 15% of Ips. No ringing 100 nanoseconds after start of pulse

Note 4: Optional, only needed if testing performed above 4000V.

Requirement:

8. I_r The maximum allowable peak-to-peak ringing must be less than 15% of I_{ps}, when measured parallel to the current waveform, with no observable ringing 100 nanoseconds after the start of the pulse.

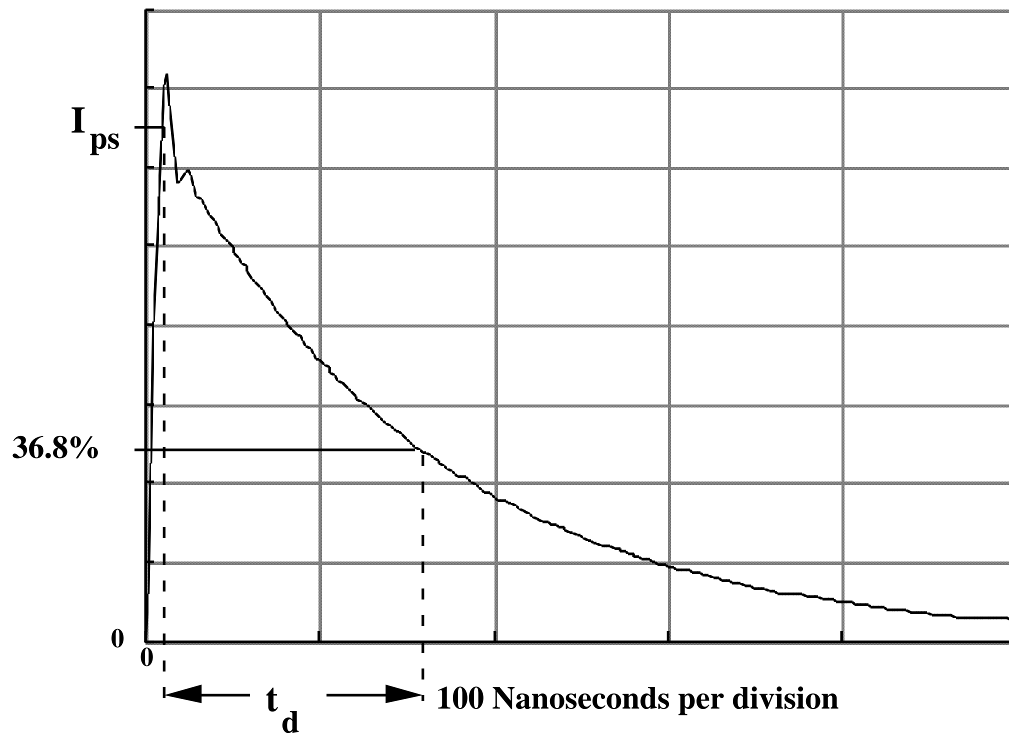


Figure 2b-Current waveform through a shorting wire (t_d)

Parameter	Value
t_d (pulse duration)	150 nanoseconds ± 20 nanoseconds

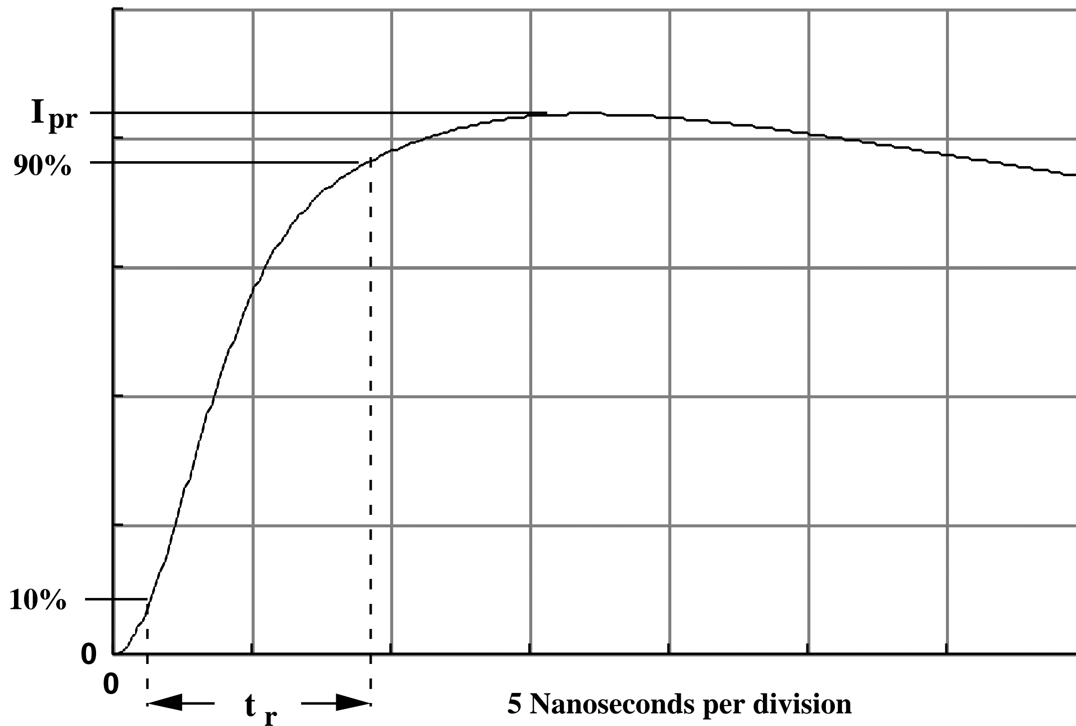


Figure 3- Current waveform through a 500 ohm resistor

Parameter	Value
I_{PR} (ampere)	375 mA – 550mA for 1000 volt pre-charge
I_{PR} (ampere)	1.5 A – 2.2 A for 4000 volt pre-charge
I_{PR}/I_{PS}	≥ 63%

Requirement:

9. The current pulse shall meet the following characteristics:

t_r Pulse rise time 5 nanoseconds to 25 nanoseconds.

I_r The maximum allowable peak-to-peak ringing must be less than 15% of I_{pr}, when measured parallel to the current waveform, with no observable ringing 100 nanoseconds after the start of the pulse.

I_{pr} Peak current through the 500 ohm resistor shall be between 375mA and 550mA for a pre-charge voltage of 1000 Volts and between 1.5A and 2.2A for a pre-charge voltage of 4000V. I_{pr} shall not be less than 63% of the previously measured I_{ps} value for the same stress level.

Notes:

5. The peak current and risetime into the 500 ohm resistor will vary, depending upon the capacitive loading of the socket and peripheral wiring.

6. It is not necessary to measure td, pulse decay time of the current through the 500 ohm resistor, as this will vary, depending upon how the tester forms the pulse.

7. The 500 ohm waveform standard is intended to assure that socket capacitance is limited. But for a given component, socket capacitance within those limits could still influence ESD withstand voltage.

Appendix A: Example of pin combinations using Table 2.

The following example is intended to clarify the pin combinations given in Table 2. The example is for a 10 pin device with 2-Vdd, 2-Vss, 2-Vcc, 2-input and 2-output pins. It is assumed that the like-named power supply pins are metallically connected. If not, each should be treated as an individual supply pin.

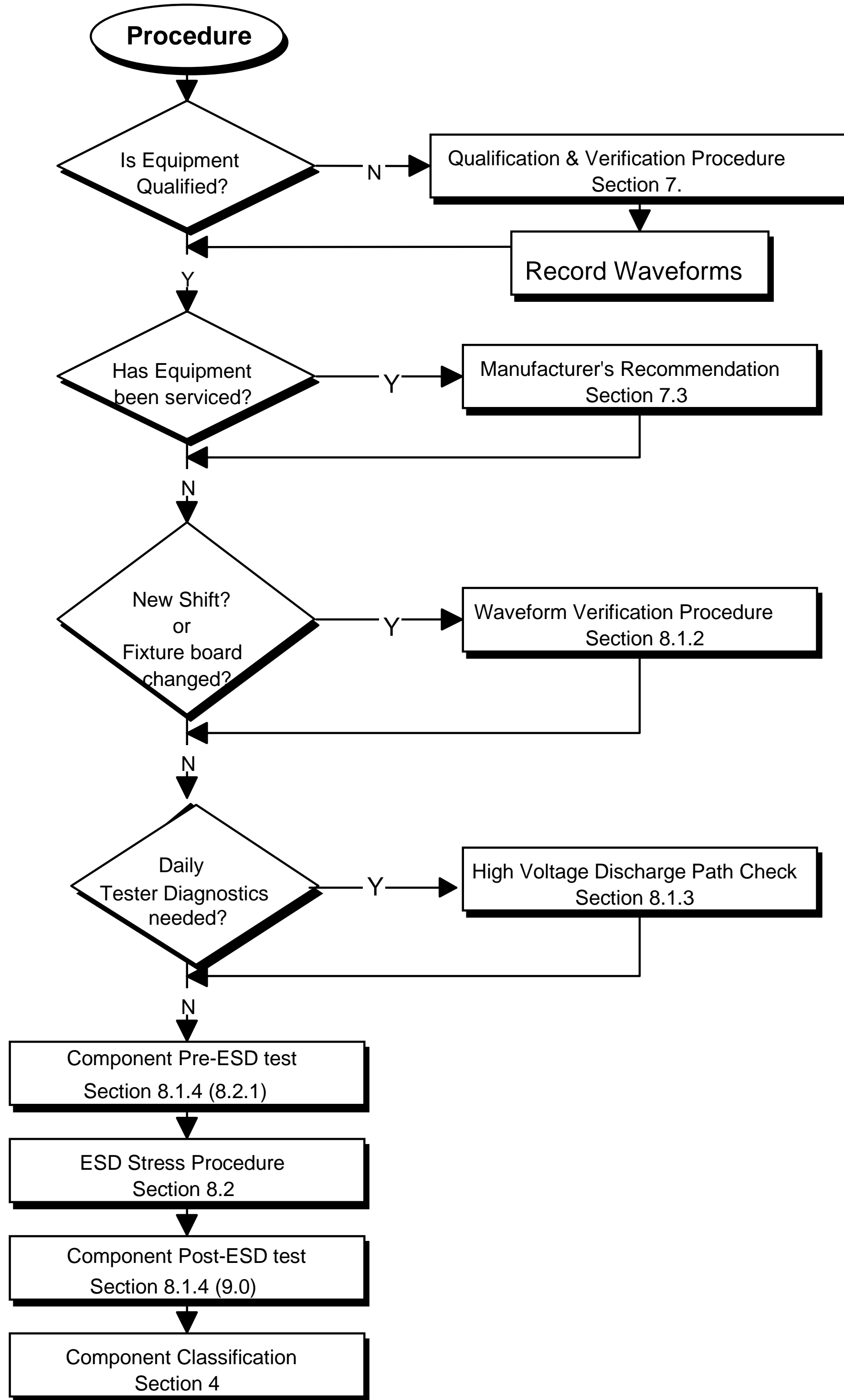
Sequence #	Pin comb.	Connect to A	Connect to B	Float Pins
1	1	1st input pin	2-Vdd	all other 7 pins
2	1	2nd input pin	2-Vdd	all other 7 pins
3	1	1st output pin	2-Vdd	all other 7 pins
4	1	2nd output pin	2-Vdd	all other 7 pins
5	1	1st Vcc pin	2-Vdd	all other 7 pins
6	1	2nd Vcc pin	2-Vdd	all other 7 pins
7	1	1st Vss pin	2-Vdd	all other 7 pins
8	1	2nd Vss pin	2-Vdd	all other 7 pins
9	2	Repeat 1-8	but swap	Vdd and Vss
10	3	Repeat 1-8	but swap	Vdd and Vcc
11	4	1st input pin	output 1,2 and input 2	all Vdd, Vss and Vcc pins
12	4	2nd input pin	output 1,2 and input 1	all Vdd, Vss and Vcc pins
13	4	1st output pin	input 1,2 and output 2	all Vdd, Vss and Vcc pins
14	4	2nd output pin	input 1,2 and output 1	all Vdd, Vss and Vcc pins

Notes:

8. Power supply and ground pins include Vdd, Vcc, Vss, GND, Grd, +Vs, -Vs, etc. as defined in 8.1.5. Pins such as offset adjust, compensation, clocks, controls, address, data and input shall be considered non-power supply pins. For each combination sequence, follow the procedure established in Section 8.2.

9. The sequence # noted, refers to the sequence of pin combinations for stressing.

Appendix B: HBM STM5.1 Procedure Flow



Bibliography

MIL-STD-883D: Test Methods and Procedures for Microelectronics: Method 3015.7 Electrostatic Discharge Sensitivity Classification.

MIL-STD-750C Notice 4: Test Methods for Semiconductor Devices: Method 1020: Electrostatic Discharge Sensitivity Classification.